ELIMINATION OF NATURAL HARMONICS IN SQUARE WAVE INVERTER

[1]Mr. N. Srinivasa reddy [2]Mr. K. Sudha Krishna [3]Mr. D. Yasin [4]Mr. G. Pulisekhar [5]Mr. S. Venkat Rami Reddy
[6]Mr. P.S. Praveen kumar   [7]Mr. K. Jagadeesh

[123456] UG Student, G. Pullaiah College of Engineering and Technology
[7] Assistant Professor, G. Pullaiah College of Engineering and Technology

Abstract – Normally, high power voltage source inverters are very common in industry and they need to provide sinusoidal output to the load for proficient operation. Sinusoidal wave output can be obtained in inverters by adopting various modulation techniques, which increases the switching frequency of the inverter elements like IGBTs and Power MOSFETs ( ), which are having limited power handling capabilities. In case of moderate to high power output from the inverter, SCRs or GTOs need to be used as inverter switching elements. These devices are having limited switching frequencies making the inverter operation impossible using the high frequency modulation techniques. This results in an output with rich harmonic content. The latest multilevel inverters can be used to overcome these problems. But the circuits very complex and also requires isolated power supplies to feed the inverter. In the proposed project, a low frequency square wave inverter using SCRs is operated along with a series connected pulse width modulated inverter, in each phase is designed. The 3-phase SCR inverter basically works as a voltage source inverter producing square wave output. The series compensator used in each phase produce only the desired harmonic voltages to make the net output voltage sinusoidal, with small PWM switching harmonics only. The series compensators are designed using the IGBTs, forming abridge inverter configuration.

Keywords – AC Motor Drives, Power Conversion, Power Conversion Harmonics

I. INTRODUCTION

The Three-Phase two-level pulse width modulation (PWM) inverter is a highly preferred scheme as a voltage source inverter for various applications. To make this inverter output voltage sinusoidal, a simple L-C filter is normally introduced at the output of this PWM inverter. For high-power applications, the switching frequency of the two-level inverters is very much restricted due to the limitation of the available power devices. This introduces increased harmonic current at the load. It also demands bigger size of the $L–C$ filter to obtain sinusoidal voltage at the output. For special applications like high-speed motor drive, where the fundamental base frequency of the voltage source can be as high as 1 kHz, PWM control of the inverter is a difficult proposition. This is again due to the limitation of the switching devices like insulated-gate bipolar transistors (IGBTs).

In these problems are tackled by various multilevel topologies.In this paper, a variant of series-connected converters and its control strategy are proposed for sinusoidal output. The basic three-phase high-voltage inverter works in square-wave mode.   But the series-connected inverters produce only the harmonic voltages using carrier-based PWM strategies, unlike all other papers mentioned before. The net output voltage has only the fundamental component with relatively small switching harmonics.

II.   METHODS OF MULTILEVEL INVERTER TOPOLOGIES

Basically there are three methods of multilevel topologies those are which are given below

1.cascaded H-bridge multilevel inverter
2.diode clamped multilevel inverter
3.capacitor clamped multilevel inverter

For the above three methods cascaded H-bridge multilevel inverter is used because of their advantages

cascaded H-bridge multilevel inverter .Theyconsist of switching devices and diodes arranged in H bridge configuration. Changing thepattern of switches for obtaining different voltage levels. .The usal inverter topology uses separate dc sources but another topology using only single dc source is also available.
Advantages:

1.we get same switching frequencies for all the switches.

2.Modular structure is easier to analyze.
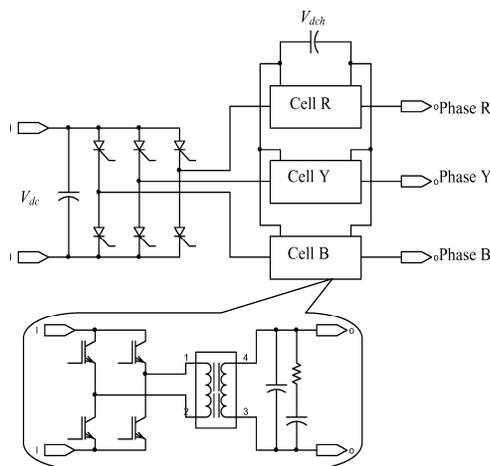
Disadvantages:

1.separate dc sources are required.

Fig 1 : Basic Converter Topology

III. DIFFERENT VARIATIONS OF THE TOPOLOGY AND THEIR CONTROL

Single-phase transformers of the series compensator are bulky. They introduce losses and also increase the cost of the system. So, the transformer less counterpart of this topology is as shown in Fig. 2. Each phase series compensator has independent dc bus. However, the size of the dc bus capacitor is needed to be high. Equation still holds good for power balance with the exception that the power absorbed by each compensator is P_{nh}.
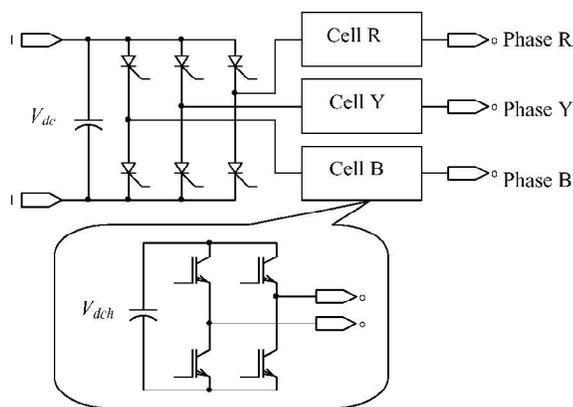

Fig 2 : Transformerless Operation of the Converter

Hence, in steady state, all three independent dc buses become $V_{dc}/2$. The load voltage V_{load} also becomes sinusoidal with small switching harmonics of the series compensator.

For the medium-voltage application, the upper limit of V_{dc} could be 2.2 kV for the PWM switching of the series compensator with dc bus voltage $V_{dc}/2$, i.e., 1.1 kV . At this limit, the rating of the IGBT for the series compensator may be at least 1700 V. Therefore, the proposed topology presented in Fig. 2 is to handle the higher level of voltages. In this topology, several single-phase full-bridge inverter cells are connected in series similar to multicell topologies . Each cell handles only one harmonic component and is named as nth harmonic cell Modulation depth "m" is taken as 1 for all the cells.

Hence, in steady state, the dc bus voltage of the nth harmonic cell becomes $2V_{dc}/n\pi$. Therefore, each cell dc bus voltage will differ from the other cell. The highest dc bus voltage is required for the lowest harmonic, i.e., fifth harmonic here. The higher harmonics will require lower dc bus voltages. This enables having higher switching frequency for higher harmonics. Assuming that the dc bus voltage of the fifth harmonic cell is limited to 1.1 kV for PWM operation, the other cell voltages and the main square-wave converter voltages are summed up in Table I.

Different Cell Voltages Of The Proposed Converter For Typical 6.6kv Applications

dc bus voltage 5th harmonic cell	dc bus voltage 7th harmonic cell	dc bus voltage 11th harmonic cell	dc bus voltage 13th harmonic cell	dc bus voltage square wave inverter	Output fundamental rms line to line voltage
1.1 KV	0.79 KV	0.50 KV	0.42 KV	8.64 KV	6.74 KV

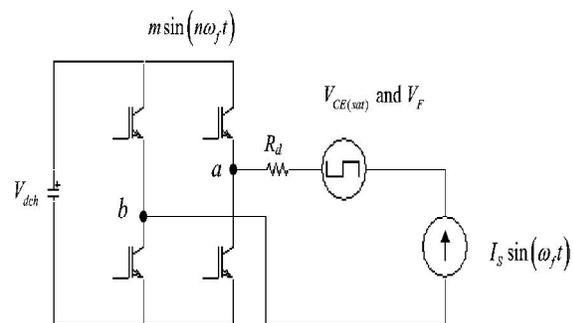### IV. PRACTICAL ISSUES OF LOSSES IN THE SERIES COMPENSATORS

Fig3: Equivalent Circuit Of Each Harmonic Cell For Loss Estimation

The analysis presented in the earlier sections is assumed to have zero losses in the series compensator. However, the

practical converters have the switching and the conduction losses. An approximate equivalent circuit of each harmonic cell is shown in Fig. 3. In steady state, the series compensator current is mostly dominated by the fundamental component of current. This is represented by a current source $I_S \sin (\omega_f t)$ in Fig. 3.In this equivalent circuit, the $V_{CE(sat)}$ (or V_F) drop of the IGBT switches (or the anti parallel diodes) can be approximately represented by a square-wave voltage signal whose fundamental frequency is same as that of the series compensator current. This square-wave voltage is also in phase with the series compensator current $I_S \sin (\omega_f t)$. In case of a MOSFET-based compensator, the drain resistances (R_d) can be represented as shown in Fig. 3.Now, the actual switches shown in fig.3. have only the non ideal switchings but no conduction drops. For ideal switching, the voltage at port a–b (V_{ab}) in Fig. 3 is mainly $mV_{dch} \sin (n\omega_f t)$and the switching harmonics. Therefore, there is no net active power transfer across the port a–b. Hence, the current source, i.e., the main square-wave inverter delivers the complete conduction losses of each harmonic cell.

Due to non ideal switchings, V_{ab} has the additional harmonic components of "$n\omega_f$" and a small amount of voltage having frequency ω_f due to the current source. This small voltage also is in phase with this current source $I_S \sin (\omega_f t)$. Therefore, there is a small amount of net active power transfer from the current source, i.e., the main square-wave inverter to the compensator across this port a–b. This small active power shares the switching losses of the compensator. Depending upon the device switching characteristics, the compensator dc bus V_{dch} also shares the switching losses. Moreover, half of the total switching per fundamental cycle ($1/\omega_f$) is soft switching (ZVS). Therefore, the net power loss (P_{sw}) at the compensator dc bus (V_{dch}) consists of small amount of device switching power loss only. Thus, asmall amount of active power is required to be drawn by this compensator to maintain its dc bus voltage V_{dch} in steady state.For the simplification, this switching power loss (P_{sw}) can be assumed to be proportional to V_{dch}. In steady state, P_{sw} should
be equal to the active power due to nth harmonic for nth harmonic cell.

V.   SIMULATION RESULTS

The proposed strategies are simulated to validate the performances. The converter configuration presented in Fig. 1 is simulated on SIMULINK platform. The fixed dc bus voltage of the square-wave inverter is 600 V. It operates in 180◦ conduction mode. The PWM switching frequency of the compensator is 5 kHz. A small ac capacitor is connected at the output of the single-phase transformer of the compensator (Fig. 1) to remove the switching ripple from the load voltage. This converter is connected to a three-phase load. This load

consists of a voltage source of 415 V L–L and has series impedance of 0.5 Ω resistance and 180 μH inductance. This converter output voltage is required to be sinusoidal.

The configuration shown in Fig. 2 is also simulated for four cells connected in series with the square-wave inverter. Unlike the previous case, the modulating signals for all the cells are sinusoidal and the modulation depths are 1. The frequency of the nth harmonic cell is the nth harmonic of the fundamental frequency of the square-wave inverter, as shown in Fig. 6. The fixed dc bus voltage of the square-wave inverter is 4400 V. The load has emf source of line-to-line rms voltage 3300 V and has series impedance of 0.2 Ω resistance and 360 μH inductance.
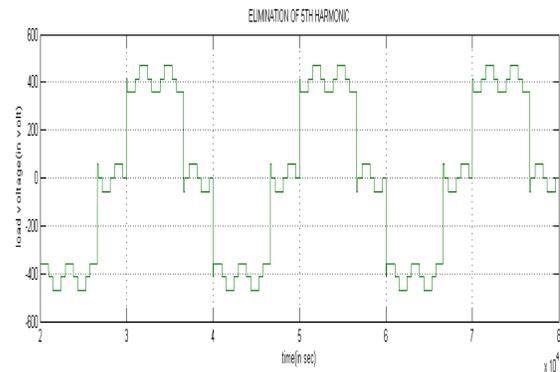

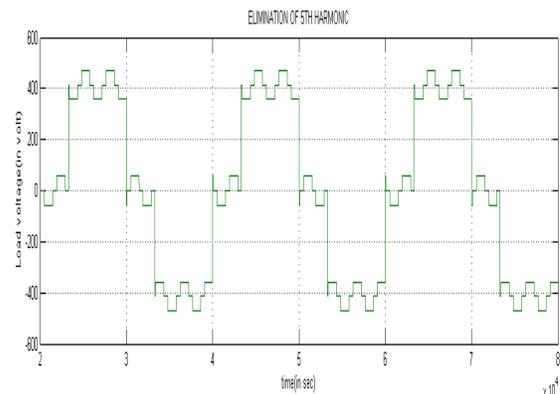*Fig4(a) : Load voltage at steady state*

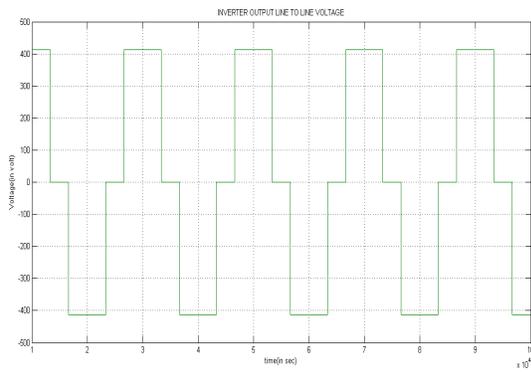*Fig4(b) : Load voltage at steady state*

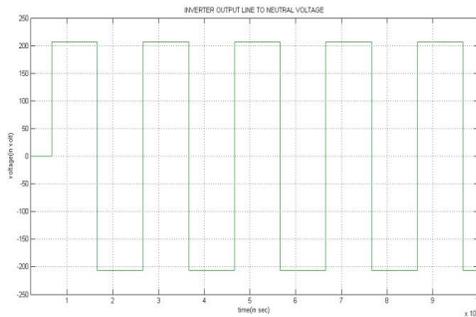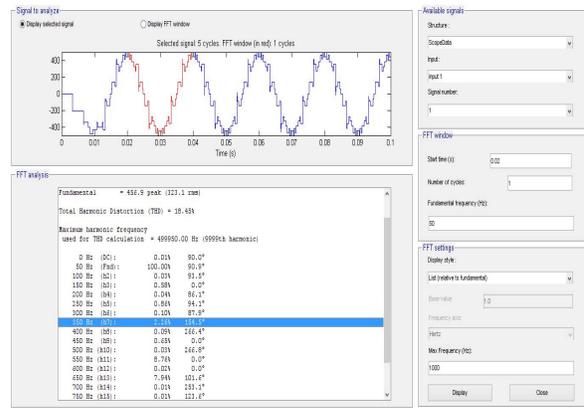*Fig4(c) : Inverter output line to line voltage*

Fig4(d) : Inverter output line to neutral voltage

VII.   CONCLUSION

In this paper, an open-loop natural control of voltage source inverter has been proposed mainly for high-power applications. The main square-wave inverter is built with high-voltage low switching-frequency semiconductor devices like integrated gate commutated   thyristors (IGCTs). The series compensators are IGBT-based inverters and operate from relatively low dc bus voltages at high switching frequencies. The series compensators produce only the desired harmonic voltages to make the net output voltage sinusoidal. For medium-voltage application, several compensating PWM inverters are connected in series. Each cell compensates one particular harmonic only. As the order of harmonic s increases, the required dc bus voltage level drops. This enables to exploit higher switching frequency for higher order harmonic cell. It has been established both theoretically and experimentally that the dc bus of the compensators do not require any external dc source or closed-loop controller for this proposed strategy. The active power at harmonic frequencies keeps the compensator dc bus voltage charged. For variable-speed drives applications, the magnitude of the fundamental output voltage should be controlled by regulating the dc bus voltage of the square-wave inverter. For static synchronous compensator (STATCOM) applications, the limited variation of this dc bus voltage may also be required. This can be achieved by drawing small active power at fundamental frequency from the grid.

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Corresponding Author: Mr. N. Srinivasa Reddy, G. Pullaian College of Engineering and Technology, India.   **1107**