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IMPLEMENTATION OF BLSEPIC CONVERTER FED BLDC MOTOR DRIVE WITH POWER FACTOR RECTIFICATION

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Abstract *- This paper presents a new technique to drive a PMBLDC motor with unipolar current, design of front end BLSEPIC and a switch which is connected in series to each phase is proposed. For the simplification of the gate drives, all switches are ground referenced. For better current regulation, the available input voltage can be boosted that is the main advantage for low voltage application. The discontinuous conduction mode of operation with an ac supply is provided to operate the SEPIC converter. Due to this mode of operation, up to an certain extent the line current follows the voltage waveform. Without the need of any voltage or current sensors, the lower order harmonics had reduced and the power factor is improved. For many variable speed drive application, the proposed topology makes simple and the parts count are reduced which is the major advantage for low cost choice and is performance are shown with the help of MATLAB / SIMULINK Software.*

Keywords- BLDC motor, DCM, PFC, bridgeless SEPIC, power-quality.

I. INTRODUCTION

A Brushless DC motor (BLDCM) possesses many advantages such as high efficiency, silent operation, varied speed range and low maintenance requirements. It is a kind of three phase synchronous motor with permanent magnets (PMs) on the rotor and trapezoidal back EMF is obtained [1-4]. It requires a three-phase voltage source inverter (VSI) as shown in figure 1 to be operated as an electronic commutator based on the rotor position signals of the BLDC obtained using Hall Effect Sensors. The three-phase VSI of the BLDC drive is fed from single-phase AC mains through a diode bridge rectifier followed by a smoothening DC capacitor, which draws an uncontrolled charging current for the DC capacitor resulting in a pulsed current. So, many power quality (PQ) problems arise such as poor power factor (PF), high Total Harmonic Distortion (THD) of AC mains current and its high crest factor (CF). Moreover, there are many international PQ standards such as IEC 61000, IEEE 519 etc [5]. Which emphasize on low harmonic contents and near unity PF current to be drawn from AC mains by various loads Therefore, an improved power quality converter based drive is almost essential for the BLDC [6]. There has been some efforts for use of power factor correction(PFC) converters for the power quality enhancement, however it uses, a two-stage PFC drives which consist of a boost converter for PFC at front-end followed by another DC – DC converter in second stage for voltage regulation. At second stage usually a fly back or a forward converter has been used for low power application and a full-bridge converter for higher power applications [7]. A Single Ended Primary Inductor Converter (SEPIC), as a single stage PFC converter, is proposed for Power Factor Correction in a BLDC motor [16].

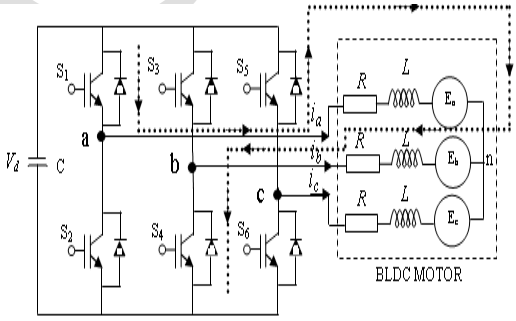

Fig 1 : BLDC Motor Drive with Inverter

II. PROPOSED CONTROL SCHEME FOR BRIDGLESS PFC CONVERTER

Bridgeless PFC topologies are currently gaining interests generally,due to the difficulty of implementation and control of bridgeless PFC converters, but a bridgeless topology can reduce conduction losses from rectifying bridges with overall system efficiency can be increased, with a bridgeless topology has the advantage of Total Harmonic Distortion (THD) decreasing from input diode reduction. The bridgeless converter circuit shown in fig 2 is typically popular for bridgeless topologies, in which the converter operates separately over positive and negative cycles. This circuit is simple and easy to implement, therefore there are fewer limitations to choosing the main passive components.

This circuit can be adapted into a single-switch bridgeless converter, which has low conduction loss and requires fewer components.

2.1 Power Stage Specification

The power stage specification of the bridgeless SEPIC PFC converter, as shown in table 1, is designed with following power stage specification:

Table 1

Input voltage, Vg	115-230V_{rms} at 50Hz
L_1	150uH
L_2 and L_3	70uH
Bulk capacitor, C_{B1} & C_{B2}	1uF
Output voltage, Vout	50V DC
Switching frequency, f_S	50kHz
Rated output power, Po	100W
Output capacitor, C_O	1410uF

2.2 Components Selections

The components were selected according to the following rationale.

- Energy transfer capacitor C1: 0.47µF
- The two inductors current ripple steering effect depends on the C1 capacitance
- Output capacitor Co: 3mF
- The magnitude of the regulated output voltage ripple is decided by the C2 capacitance.
- Input inductor L1 & output inductor L2: 600µH
- The size of the inductor current ripple is decided by the L1 inductance.

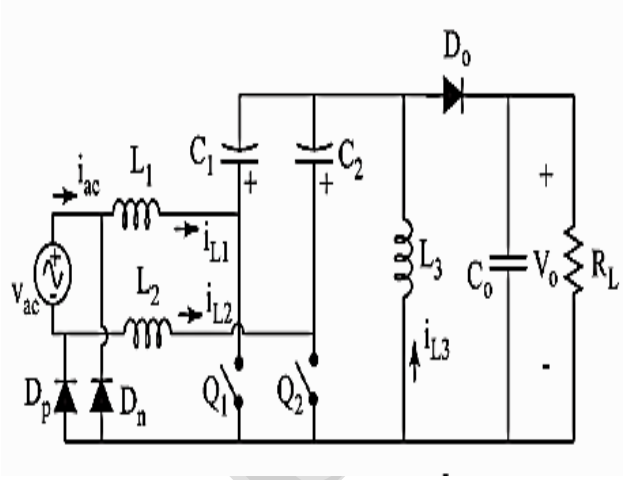

Fig 2 : Control scheme of the proposed Bridgeless SEPIC converter

III. MODELING OF BRIDGELESS SEPIC PFC CONVERTER

3.1 Bridgeless SEPIC Converter Model

The single-switch bridgeless SEPIC PFC converter has only one active switch that makes the topology simple,butthe modelling is complicated with the two inductors and two capacitors. Fig 3(a) and 3 (b) depict the operations for each cycle of the switch on-time and the switch off-time in the positive half cycle. L1 only conducted during the positive half cycle, and L2 is left uncontrolled. Even though the desired sensing current is the only current through L1, the actual sensing current is the sum of currents flowing into L1 and L2. The current flowing in L2 creates an undesired ripple of the sensed current during positive half line cycle.

Inductances of L1 and L2 should be selected with consideration of these ripples. Alternativedifference of this topology is the undesired circulating current from the capacitive coupling loop, as shown in fig 3 (a) and (b). The circulating current causes power loss but does not significantly affects the total efficiency, so, in this it will not be considered. Although the two features mentioned above affect the system performance, thus the effects are not significantly impact the model of the system. Thus, the input and output voltage is considered to be constant voltages due to the exploration of the small-signal linear model which was performed while assuming a quasi-static condition, because the switching frequency is much higher than the line frequency.

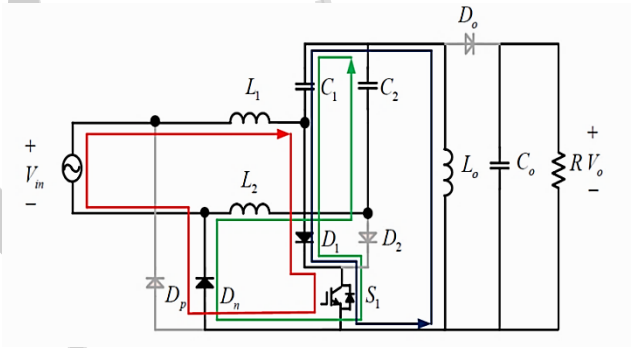

Fig 3 :. (a) Bridgeless SEPIC PFC Converter (switch-on).

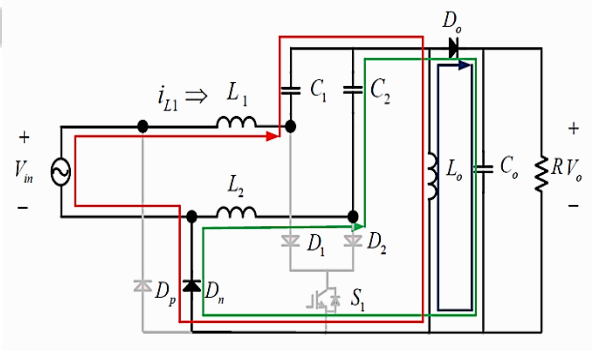

Fig 3 : (b) Bridgeless SEPIC PFC Converter (switch-off).

3.2 Switch on Stage of SEPIC Converter

In MODE 1, the equivalent circuit is shown in Fig (4). As can be seen, when the upper MOSFET, S1, is turned on,the current from the source, Vg, will flow through the inputinductor and continue to S1 and Ds2 before completing thecurrent path through Vg. At the same time, as shown inFigure 4, the current through L1 increased linearly to its peakvalue,

$$i_{L1-peak} = \frac{v_g}{L_1}(d_1 T_S)$$

where d1 is the duty cycle. On the other hand, the second inductor, L2 discharged its energy linearly to Cb1 and createsa current path to MOSFET S1 before returning to L2. It is found that the current flowing through S1 is the addition of the current through L1 and L2. At this point, the output voltage is equal to the capacitor voltage, Vo, due to output diode, Do1 being reverse-biased.

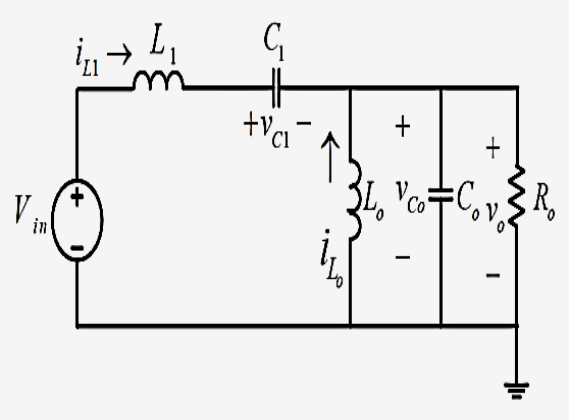

Fig 4 : Operation of the SEPIC Converter Switch On-Stage.

3.3 Switch-Off stage of SEPIC Converter

Fig 5 shows the circuit in MODE 2. Obviously at this mode, S1 is turned off such that no current will flow through it, but now Do1 is forward-biased. At this point, together with Vg, the current through L1 falls linearly due to the process of discharging its current to the load through iCb1 and iDo1 and create the return path through Ds2. At the same time, L2 will also discharge its current linearly to the load through iDo1. Now, the current flowing through Do1 is the summation of iL1 and iL2. Thus, the peak current for Do1 is

$$i_{Do1-pk} = d_1 T_S \left(\frac{v_g}{L_a} \right)$$

where La = L1//L2. In addition, the peak current flowing through MOSFET S1 is exactly the same with Do1 due to the summation of current at L1 and L2.

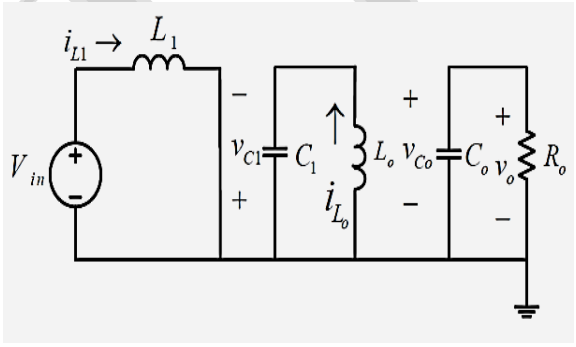

Fig 5 : Operation of the SEPIC Converter Switch Off-Stage.

A stabilized system is not easy to achieve with a second resonance point due to the significant high quality-factor of it. The un-damped resonance causes oscillations in the input current with the same frequency of the second resonance point. The oscillating current makes the system unstable as shown in fig 6.

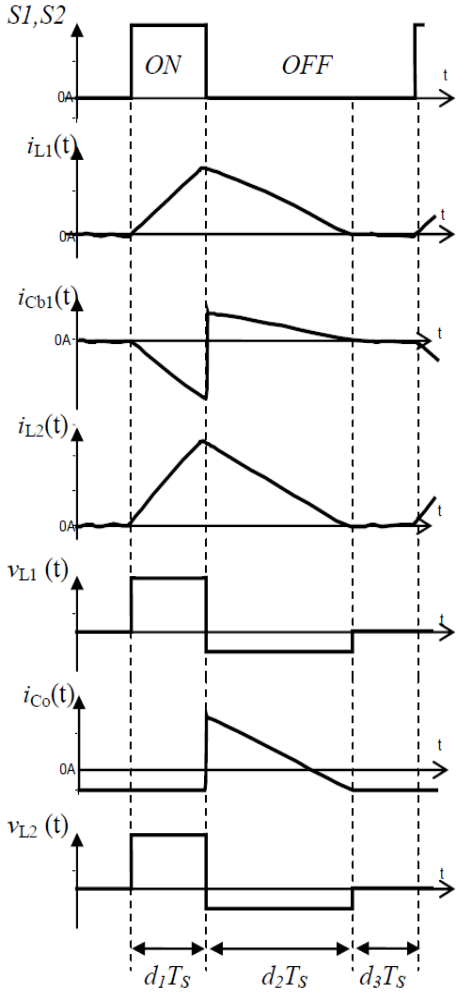

Fig 6 : Waveforms within each switching period for several components.

IV. SIMULATION RESULT

The proposed BLDCM drive is modelled in Matlab-Simulink environment and its performance is evaluated with load The DC link voltage is kept constant at 400 V with an input AC RMS voltage of 225V. The components of SEPIC converter are selected on the basis of power quality constraints at supply mains and allowable ripple in DC-link voltage as discussed as shown in Fig 7.

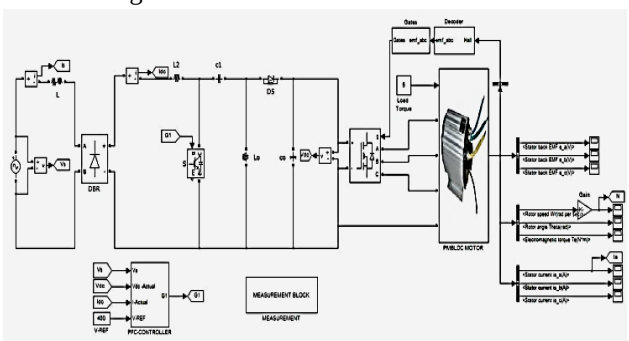

Fig 7 : Simulation Diagram of the Proposed Circuit

The controller gains are tuned to get the desired power quality parameters. The performance evaluation is made on the basis of various power quality parameters i.e. total harmonic distortion of current (THD %) at input AC mains, power factor (PF) and input AC current (Is). Figure 6 shows the current (I) waveform at input AC mains is in phase with the supply voltage (Vs) representing nearly unity power factor. The waveforms of power factor of BLDC motor drive are shown in Figure-8.Performance of the proposed BLDC motor drive is evaluated under varying input AC voltage todemonstrate the effectiveness of the proposed in various practical situations in Table-2.

Table:2 PQ Parameters of a BLDCM at VariableInput AC Voltage

(Vs)	(Is)	RPM	(THD %)	(PF)
300	3.712	1350	1.95	0.9992
270	3.342	1240	1.72	0.9987
210	1050	1050	1.32	0.9986
180	2.229	910	1.11	0.9985
120	1.486	690	0.98	0.9984
90	1.114	560	0.89	0.9985
60	0.724	380	1.25	0.9985
30	0.371	230	0.96	0.9985

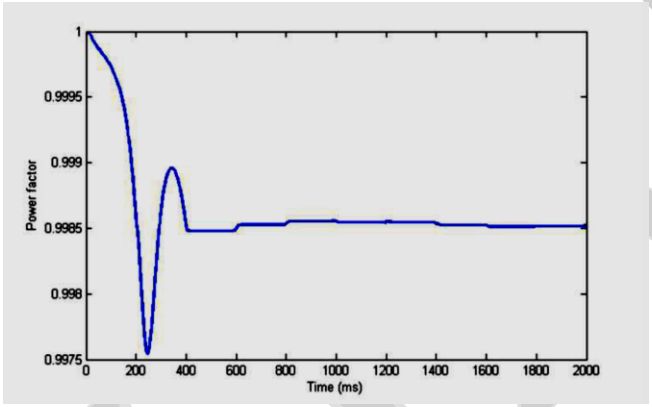

Fig 8 : Power factor of the BLDC motor at peak source voltage of 240V

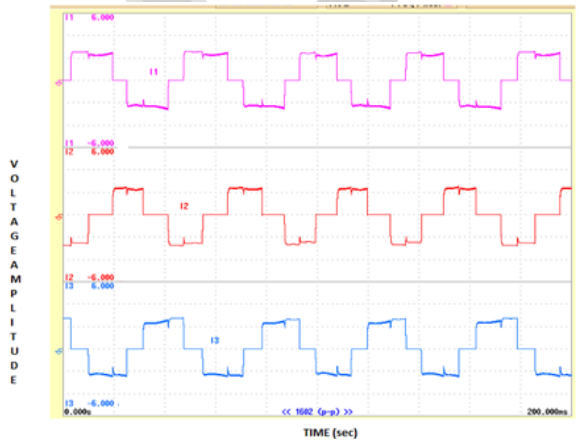

Fig 9 : (a) Phase Voltage of BLDC Motor

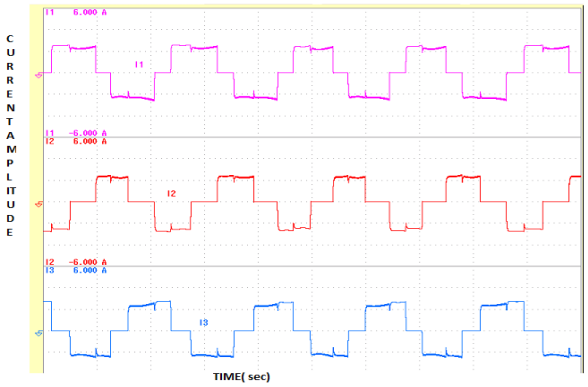

Fig 9 : (b) Phase Current of BLDC Motor

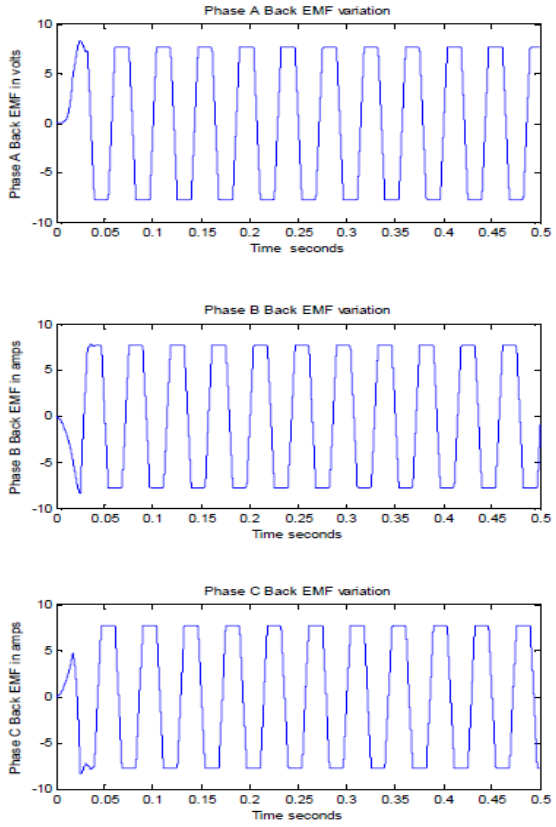

Fig 10 : Trapezoidal back emf of the BLDC motor

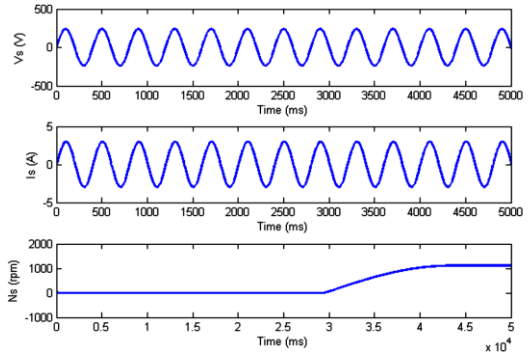

Fig 11 : Performance of the PMBLDCM drive at peak source voltage of 240V

Fig 9-11 show variation of current and its THD at ACmains with AC input voltage. The total harmonic distortions of AC

mains current is observed well below 5% in most of the cases and satisfies the international standards along with nearly unity PF in wide range of AC input voltage.

V. CONCLUSION

By using a voltage follower approach, a simple control is implemented in this paper to control the voltage and power factor is corrected for a BLDC Motor drive with PFC BLSEPIC Converter. For a wide speed range, the power quality is improved at AC mains and also the speed control is achieved by the design of single stage PFC converter system. To demonstrate the effectiveness of the proposed topology, the evaluation is undergone under various input AC voltage on MATLAB / SIMULINK Software which shows the performance improvement of the BLDC Motor drive.

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